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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,048	06/19/2003	Louis A. Lippincott	884.899US1	6019

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EXAMINER

NGUYEN, HAU H

ART UNIT	PAPER NUMBER
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2628

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/600,048

Applicant(s)

LIPPINCOTT, LOUIS A.

Examiner

Hau H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to Applicants' Request for Continued Examination (RCE), filed August 2, 2006. Claims 1-30 remain in this Application. As a result of Applicants' RCE, a new search has been performed. Rejections based on the newly cited references follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Tulpule et al. (U.S. Patent No. 4,933,836, hereinafter, Tulpule).

As per claim 1, Tulpule teach a first processor 12 (Fig. 1) having two or more processor elements (Fig. 7, col. 13, ll. 32-48), and two or more input/output ports coupled together by a first port ring this is within the first processor (Fig. 2, col. 8, ll. 34-40); and a second processor 18, which is similar to the first processor 12, couples to the first processor 12 through at least one I/O port of a third port ring within a third processor 14 (Fig. 1).

As per claim 2, as shown in Fig. 1, Tulpule, teach the two or more I/O ports of the first processor is not directly connected to the two or more I/O ports of the second processor.

Claim Rejections - 35 USC § 103

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-12, 18-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836) in view of Galicki et al. (U.S. Patent No. 6,967,950, hereinafter, Galicki).

As per claims 3, Tulpule fails to teach the first, second, and third processors are part of a number of processors in a point-to-point configuration. However, Galicki et al. teach a method of transferring data between multiple digital signal processors from the source processor 201 to the destination processor in a point-to-point configuration (Fig. 2, col. 4, ll. 45-55).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Galicki in combination with the method as taught by Tulpule in order to increase system performance, simplifies software and decreases central processing unit and direct memory access unit loading (col. 3, ll. 10-20).

As per claim 4, although Tulpule does not explicitly teach the first processor transmitting output from an image process operation to the second processor, Tulpule does teach the processors are the signal processors, and also suggest using for image processing (col. 1, ll. 61-68). Although Tulpule fails to teach transmitting of image data to the second processor from the first processor based on a logical connection, Galicki teaches this feature as cited above (implemented via the datapipe).

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As per claim 5, although Tulpule fails to explicitly teach the I/O ports of the processors comprising a FIFO memory, Tulpule does teach at the I/O ports of the signal processor 12 (such as “North” and “South” ports, Fig. 3) comprising a dual port RAM 74 and 76 to communicate with other modular entities (col. 10, ll. 36-41). Therefore, it would have been obvious to one skilled in the art to modify the memories 74 and 76 into FIFO in order to queue the commands received or transmitted at each processor.

As per claim 6, Tulpule does not explicitly teach the I/O ports of each processor comprising a transmitter port and receiver port, wherein the first processor configured to transmit the output based a handshake protocol among the receiver ports and the transmitter ports of the first processor, the second processor, and the third processor. However, this is taught by Galicki with reference to Figs. 10 and 11.

As per claim 7, as cited above, the teachings of Tulpule and Galicki in combination teach the limitations of claim 7. Specifically, Tulpule teach a plurality of signal processors 12-18, each includes plurality of I/O ports configured in a port ring, at least one signal processor 24, which may be used in image processing, wherein one signal processor coupled to another signal processor via the I/O ports of the port rings. Galicki teach the digital signal processors are coupled together in a point-to-point configuration.

As per claim 8, the combined system teaches the at least one processor element in a first of the number of image processors is configured to perform one of a number of image processed-based operations.

Claims 9, 10, and 12, which are similar to claims 4 and 5, are thus rejected under the same rationale.

As per claim 11, although not explicitly taught by Tulpule, Galicki teach the logical connections are to originate at a source image signal processor of the number of image signal processors and to traverse a number of intermediate image signal processors of the number of image signal processors and to complete at a destination image signal processor of the number of image signal processors, wherein the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection (Fig. 5, col. 5, ll. 48-62).

Claims 18-30 are similar in scope to claims 6-12, and thus are rejected under similar rationale.

6. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tulpule et al. (U.S. Patent No. 4,933,836) in view of Galicki et al. (U.S. Patent No. 6,967,950), and further in view of Hsieh et al. (U.S. Patent No. 6,757,019, hereinafter, Hsieh).

As per claim 13, the teachings of Tulpule and Galicki are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach or suggest a CMOS sensor to capture image data. This is what Hsieh teaches. As shown in Figs. 3 and 4, Hsieh teaches an image processor including a plurality of image signals processors 40, having a plurality of expansion interfaces (DMA 50, Fig. 5) configured to receive the image data to captured by the CMOS sensor 22 (col. 5, ll. 1-14). Hsieh also teaches the host processor configure a number of logical connection among the number of image signal processors 40 (Figs. 2A-2C, col. 4, ll. 13-24).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Hsieh in combination with the method as taught by Tulpule and Galicki because CMOS image sensor provides high speed video capturing and thus further increase the overall image processing performance. Therefore, at least claim 13 would have been obvious.

As per claim 14, the combined system provides at least one image signal processor comprises a hardware accelerator (such as signal processor, Tulpule, or PEs 40, of Hsieh) to execute image process operations.

As per claim 15, Hsieh teaches the image processor comprises a global bus (such as, bus connects the PEs as shown in Fig. 2C) coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

Claim 16 is similar in scope to claim 11, and thus is rejected under similar rationale.

As per claim 17, Galicki teaches traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processors (Fig. 2, col. 4 12, ll. 45-55).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen

10/06/2006



KEE M. TUNG
SUPERVISORY PATENT EXAMINER